UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,302	09/10/1999	ALVAR A. DEAN	BU9-98-062	4030

29154 7590 05/23/2007

FREDERICK W. GIBB, III
Gibb & Rahman, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
CHU, GABRIEL L	

ART UNIT	PAPER NUMBER
2114	

MAIL DATE	DELIVERY MODE
05/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/394,302	DEAN ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55-70 and 97-104* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-70 and 97-104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 97-99, 101 rejected under 35 U.S.C. 102(b) as being anticipated by US 4593820 to Antonie et al.

3. Referring to claim 97, Antonie discloses transporting said IC chips; and testing said IC chips during said transporting (Abstract, "Test signals supplied through the test head will conduct real time testing of the device while it is being transported by the robot arm from the pick-up point to one of several destination receptacles.").

4. Referring to claim 98, Antonie discloses supplying power to a test circuit connected to said IC chips during said transporting (Abstract, "Test signals supplied through the test head will conduct real time testing of the device while it is being transported by the robot arm from the pick-up point to one of several destination receptacles.").

5. Referring to claim 99, Antonie discloses identifying ones of said integrated circuit chips which failed said testing (From line 23 of column 3, "By the time that the robot arm 8 has mechanically displaced the electronic device to the first receptacle 38, the test of the device will have been completed. The receptacles 38 and 40 correspond to two different test results for the device under test. If the device is determined to have a first

test result characteristic, the tester 25 will convey that information to the controller 20 and the controller 20 will then control the motors 14 and 16 to locate the tested device in the gripper assembly 15 above the receptacle 38 where it will be placed therein. Alternately, if the test results determined by the tester 25 indicate a second test result characteristic corresponding to the receptacle 40, the tester 25 will convey this information to the controller 20 and the controller 20 will then control the motors 14 and 16 to direct the placement of the gripper assembly 15 above the second receptacle 40 and the tested electronic device will be placed therein." Further, from line 3 of column 7, "The functional test being performed on the device under test can typically take place during a time interval which is less than the time interval necessary for the mechanical displacement of the device under test from the pick-up point 36 to the first receptacle 38 of FIG. 1, and therefore the tester 25 will be able to output its results to the controller 20 as is reflected by step 128 in FIG. 14, prior to the instant when the gripper assembly 15 is positioned above the first receptacle 38 of FIG. 1. Step 128 of FIG. 14 has the controller 20 processing the results of the functional testing which was performed by the tester 25. Typically, the results of a functional test on the device under test 64 will be that the device is either acceptable (a good device) or not acceptable (a bad device) based upon testing criteria previously established and programmed into the tester 25. It should be evident, however, that more than two types of test results can be obtained for testing a device under test, such as in testing memory arrays where usable contiguous sectors of a memory array are tested to be good and other sectors are tested not to be good and therefore as many as four or five test results can be obtained in such

situations. Thus, as many destination receptacles 38 and 40 can be provided as there are different test results which can be expected from the tester 25.").

6. Referring to claim 101, Antonie discloses said identifying comprises displaying a visual indicator of passing or failing chips (From line 23 of column 3, "By the time that the robot arm 8 has mechanically displaced the electronic device to the first receptacle 38, the test of the device will have been completed. The receptacles 38 and 40 correspond to two different test results for the device under test. If the device is determined to have a first test result characteristic, the tester 25 will convey that information to the controller 20 and the controller 20 will then control the motors 14 and 16 to locate the tested device in the gripper assembly 15 above the receptacle 38 where it will be placed therein. Alternately, if the test results determined by the tester 25 indicate a second test result characteristic corresponding to the receptacle 40, the tester 25 will convey this information to the controller 20 and the controller 20 will then control the motors 14 and 16 to direct the placement of the gripper assembly 15 above the second receptacle 40 and the tested electronic device will be placed therein.").

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 55-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. in view of US 4026412 to Henson.

9. Referring to claim 55, Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.); a test board in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.).

Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Although Steiner in view of Miller does not specifically disclose that the test box

surrounds the IC [see BPAI and Examiner's arguments regarding "during transportation"], covering the IC during testing is known in the art. An example of this is shown by Henson, from the abstract, "For protection of the microelectronic packages during storage and shipment, they are positioned within a carrier which encloses the body of the package and restrains the package leads for complete protection. Preferably the carrier has electrical access to the leads so that testing of the package can take place when the completed package is protected within the carrier." A person of ordinary skill in the art at the time of the invention would have been motivated to cover DUTs during test because, as shown by Henson, "encloses the body of the package and restrains the package leads for complete protection".

10. Referring to claim 56, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing

procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

11. Referring to claim 57, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

12. Referring to claim 58, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

13. Referring to claim 59, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

14. Referring to claim 60, Steiner in combination with Miller et al. disclose each of said test boards includes comparators electrically connected to said sockets (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a

comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

15. Referring to claim 61, Steiner in combination with Miller et al. disclose said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)."), and wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips (From the abstract of Miller et al., "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

16. Referring to claim 62, Steiner in combination with Miller et al. disclose said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously (From the technical field of Miller et al., "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel.").

17. Referring to claim 63, Steiner discloses a transportable integrated circuit (IC) chip test device, said device comprising: a transportable test box (See figure 1.); a test board mounted in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: sockets adapted to hold an IC chip to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.).

Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Further, although Steiner does not specifically disclose the comparison of a plurality of ICs, it is known in the art. An example of this is further shown by Miller et al. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said IC

chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.). A person of ordinary skill in the art at the time of the invention would have been motivated to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications." Further, although Steiner does not specifically disclose the test device is adapted to test application specific integrated circuits (ASICs), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester. A person of ordinary skill in the art at the time of the invention would have been motivated to test ASICs because they can be faulty.

Although Steiner in view of Miller does not specifically disclose that the test box

surrounds the IC [see BPAI and Examiner's arguments regarding "during transportation"], covering the IC during testing is known in the art. An example of this is shown by Henson, from the abstract, "For protection of the microelectronic packages during storage and shipment, they are positioned within a carrier which encloses the body of the package and restrains the package leads for complete protection. Preferably the carrier has electrical access to the leads so that testing of the package can take place when the completed package is protected within the carrier." A person of ordinary skill in the art at the time of the invention would have been motivated to cover DUTs during test because, as shown by Henson, "encloses the body of the package and restrains the package leads for complete protection".

18. Referring to claim 64, Steiner in combination with Miller et al. disclose all of said ASIC chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in parallel without altering the test program or the conventional tester.").

19. Referring to claim 65, Steiner in combination with Miller et al. disclose each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets (From line 67 of column 3 of Steiner, "When the user has operated switches 12 and 13 so that the alpha numeric word appearing in display 16 corresponds to the device plugged into socket 10, the on/test button 11 is again depressed. The preferred embodiment then performs a series of tests which will test all the relevant combinations of inputs for the unit under test and

tests for the proper outputs therefrom. If the unit under test is operating properly an appropriate message is displayed in display 16. If the unit under test fails, an indication that the UUT failed the test as well as an identification of the step in the test procedure which the unit failed will be shown in display 16. This step is of course related to the software controlling the test procedures. External documentation of the testing procedures can identify the particular input/output combination for which the unit under test failed to respond properly if this is considered important to the user.").

20. Referring to claim 66, Steiner in combination with Miller et al. disclose the portable power supply comprises a battery (From the abstract of Steiner, "A battery operated...").

21. Referring to claim 67, Steiner in combination with Miller et al. disclose each of said test boards includes a memory adapted to store test results (From line 54 of column 4 of Miller et al., "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

22. Referring to claim 68, Steiner in combination with Miller et al. disclose each of said test boards includes a known good integrated circuit chip (From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

23. Referring to claim 69, Steiner in combination with Miller et al. disclose all of said comparators are connected to known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip (From the abstract of Miller et al., "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

24. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. and US 4026412 to Henson as applied to claim 63 above, and further in view of US 6499121 to Roy et al.

25. Referring to claim 70, although Steiner in combination with Miller and Henson do not specifically disclose by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested, testing without a known output is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors

on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the

interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a portable circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

26. Claim 100 rejected under 35 U.S.C. 103(a) as being unpatentable over US 4593820 to Antonie et al. as applied to claim 99 above, and further in view of "storing test results in memory".

27. Referring to claim 100, Antonie discloses test results (From line 23 of column 3, "By the time that the robot arm 8 has mechanically displaced the electronic device to the first receptacle 38, the test of the device will have been completed. The receptacles 38 and 40 correspond to two different test results for the device under test. If the device is determined to have a first test result characteristic, the tester 25 will convey that information to the controller 20 and the controller 20 will then control the motors 14 and 16 to locate the tested device in the gripper assembly 15 above the receptacle 38 where it will be placed therein. Alternately, if the test results determined by the tester 25

indicate a second test result characteristic corresponding to the receptacle 40, the tester 25 will convey this information to the controller 20 and the controller 20 will then control the motors 14 and 16 to direct the placement of the gripper assembly 15 above the second receptacle 40 and the tested electronic device will be placed therein." From line 3 of column 7, "The functional test being performed on the device under test can typically take place during a time interval which is less than the time interval necessary for the mechanical displacement of the device under test from the pick-up point 36 to the first receptacle 38 of FIG. 1, and therefore the tester 25 will be able to output its results to the controller 20 as is reflected by step 128 in FIG. 14, prior to the instant when the gripper assembly 15 is positioned above the first receptacle 38 of FIG. 1. Step 128 of FIG. 14 has the controller 20 processing the results of the functional testing which was performed by the tester 25. Typically, the results of a functional test on the device under test 64 will be that the device is either acceptable (a good device) or not acceptable (a bad device) based upon testing criteria previously established and programmed into the tester 25. It should be evident, however, that more than two types of test results can be obtained for testing a device under test, such as in testing memory arrays where usable contiguous sectors of a memory array are tested to be good and other sectors are tested not to be good and therefore as many as four or five test results can be obtained in such situations. Thus, as many destination receptacles 38 and 40 can be provided as there are different test results which can be expected from the tester 25.").

Although Antonie does not specifically disclose that the test results may be

stored in a memory, storing test results is notoriously well known in the art. Examiner takes official notice for "storing test results in memory". An example of this, particularly in view of above section disclosed by Antonie, is storing a memory map of failed memory locations. A person of ordinary skill in the art at the time of the invention would have been motivated to store such a map because, as disclosed by Antonie, "usable contiguous sectors of a memory array are tested to be good and other sectors are tested not to be good and therefore as many as four or five test results can be obtained in such situations."

While examiner has given the example of storing a memory map for determining good memory locations, examiner notes that storing test results need not be limited to such an embodiment and obviously be for any subsequent access step, such as so that the gripper arm of Antonie may access a test result for determining which bin to deposit a tested device into.

28. Claim 102, 103 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4593820 to Antonie et al., and further in view of US 6499121 to Roy et al.

29. Referring to claim 70, although Antonie does not specifically disclose comparing output signals of IC chips with each other, comparing whether outputs of all IC chips are identical so that testing circuitry does not require a specific proper output that a given input should produce is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the

test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT

comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into any circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

30. Referring to claim 103, although Antonie does not specifically disclose comparing output signals of one IC chip with output signals of all other IC chips that have not been identified as defective, comparing whether outputs of all IC chips are identical so that testing circuitry does not require a specific proper output that a given input should produce is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry

may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of

ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into any circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

31. Claim 104 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4593820 to Antonie et al., and further in view of US 6452411 to Miller et al.

32. Referring to claim 104, although Antonie does not specifically disclose said testing includes comparing output signals of said IC chips with a golden chip, using a known good chip to compare to identify faulty chips is known in the art. From the abstract of Miller et al., "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel." A person of ordinary skill in the art at the time of the invention would have been motivated to compare with a known good chip because Antonie has specifically disclosed the need of being able to determine a faulty chip and known good comparisons fulfills this need.

33. Claims 55, 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. in view of "covering things".

34. Referring to claim 55, Steiner discloses a transportable circuit chip test device comprising: a transportable test box (See figure 1.); a test board in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards

(From the abstract, "A battery operated..."), wherein said test board comprises: a socket adapted to hold integrated circuit chips to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.).

Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Although Steiner in view of Miller does not specifically disclose that the test box surrounds the IC [see BPAI and Examiner's arguments regarding "during transportation"], covering the IC during testing is known in the art, but generally, covering anything is well known. Examiner takes official notice for "covering things." "Covering things" has been known for some time, and can probably be traced back to our ancestors' propensity for seeking shelter from the elements. Over time, and for different applications, "covering things" has been used for different purposes but has

still been known to, quite possibly, all people on the planet. Some specific instances of "covering things" are a chip fabrication facility's being indoors, having a roof on a car with its windows rolled up all the way, a lid on a pot, a computer with its case closed, a monitor without its innards exposed, closing a printer cover after servicing (thereby enabling printing), packaging a chip, etc... A person of ordinary skill in the art at the time of the invention would have been motivated to "cover things" for a tester because of reasons such as protecting what is within from what is without (e.g., dust, the elements, hands), indicating that what is inside is under test, enabling a tester to commence testing (a la microwave door), locking what is within into position, creating the appearance of a more cohesive unit, and any other reason not explicitly referenced herein.

35. Referring to claim 63, Steiner discloses a transportable integrated circuit (IC) chip test device, said device comprising: a transportable test box (See figure 1.); a test board mounted in said test box (See figure 2.); and a portable power supply in said test box connected to said test boards (From the abstract, "A battery operated..."), wherein said test board comprises: sockets adapted to hold an IC chip to be tested while being transported (See figure 1, element 10.); and testing circuitry electrically connected to said sockets (See figure 2, element 25.).

Although Steiner does not specifically disclose a plurality of test boards and that each test board can hold more than one integrated circuit to be tested, the testing of more than one integrated circuit in a system is well known in the art. An example of this is shown by Miller et al., from the abstract, "In response, the interface circuitry writes the

data to corresponding locations in each of a number of devices under test (DUTs)." Further, from line 4 of column 2, "To increase the throughput of the test system in terms of the number of DUTs tested per unit time, a larger tester may be built with more channels." A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time".

Further, although Steiner does not specifically disclose the comparison of a plurality of ICs, it is known in the art. An example of this is further shown by Miller et al. Miller et al. disclose said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said IC chips simultaneously, and wherein said testing circuitry identifies a defective IC chip as one having a different output when compared to outputs of the other ASIC chips, when all IC chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices

using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.). A person of ordinary skill in the art at the time of the invention would have been motivated to compare DUTs in a portable tester because, from line 24 of column 1, "the manufacturer expects each constituent IC device to be virtually free of defects and to perform according to its specifications." Further, although Steiner does not specifically disclose the test device is adapted to test application specific integrated circuits (ASICs), the testing of ICs that are application specific is well known in the art. An example of this is an ASIC tester. A person of ordinary skill in the art at the time of the invention would have been motivated to test ASICs because they can be faulty.

Although Steiner in view of Miller does not specifically disclose that the test box surrounds the IC [see BPAI and Examiner's arguments regarding "during transportation"], covering the IC during testing is known in the art, but generally, covering anything is well known. Examiner takes official notice for "covering things." "Covering things" has been known for some time, and can probably be traced back to our ancestors' propensity for seeking shelter from the elements. Over time, and for different applications, "covering things" has been used for different purposes but has still been known to, quite possibly, all people on the planet. Some specific instances of "covering things" are a chip fabrication facility's being indoors, having a roof on a car with its windows rolled up all the way, a lid on a pot, a computer with its case closed, a monitor without its innards exposed, closing a printer cover after servicing (thereby enabling printing), packaging a chip, etc... A person of ordinary skill in the art at the time

of the invention would have been motivated to "cover things" for a tester because of reasons such as protecting what is within from what is without (e.g., dust, the elements, hands, etc...), protecting what is without from what is within (e.g., during electrostatic discharge testing, toxic elements, etc...), indicating that what is inside is under test, enabling a tester to commence testing (a la microwave door), locking what is within into position, creating the appearance of a more cohesive unit, and any other reason not explicitly referenced herein.

36. Claim 97 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6452411 to Miller et al. in view of "doing things while in transit".

37. Referring to claim 97, Miller discloses a method for testing IC chips (see abstract, above, etc...). Indeed, testing integrated circuit chips is a very well known activity conducted in the industry.

Although Miller does not disclose such testing may occur during the transport of the IC chips, "doing things while in transit" is generally a well known concept in modern, civilized society. Examiner takes official notice for "doing things while in transit". Examples of this can be applying make-up while driving, reading the paper on the train, talking on the phone about a business transaction in the back of a limousine, doing work in an airport or on a plane, etc... In short, it is known to use the time spent being conveyed to perform other tasks, thereby saving time and/or ensuring the task is performed as late as possible prior to arriving at a destination (such as calling a friend as you are getting close to his residence), or whatever other reason there may be for "doing things while in transit". Merely "doing things while in transit" is common

knowledge. Applicant has presented no such non-obvious solution to any problem. In fact, in specificity, as substantiated by Antonie above, testing while transporting is a known chip manufacturing efficiency. Although Antonie does not perform this, say, on the back of a truck, examiner does not believe that such a placement provides any novel, non-obvious feature, particularly as claimed by Applicant.

Conclusion

38. The plain language rejections above were given so that applicant may be apprised of the **common sensical** nature of applicant's claims; or at least the **common sensical** view examiner has of Applicant's claims. If Applicant chooses to pursue the invention, examiner suggests claims/claim language which may overcome at least such **common sense**.

39. From SCOTUS KSR v. Teleflex decision, page 5 (with emphasis), "Under the correct analysis, any need or problem known in the field and addressed by the patent can provide a reason for combining the elements in the manner claimed.... It is **common sense** that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle... When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and **common sense**... Rigid

preventative rules that deny recourse to **common sense** are neither necessary under, nor consistent with, this Court's case law."

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Primary Examiner
Art Unit 2114

gc